

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory array having at least a first area and a second area, which stores cell data, a data input circuit located
5 closer to the first area than the second area, to which the cell data is input, and an error correction circuit which generates parity data for error correction from the cell data input to the data input circuit. The device further includes a control circuit which stores
10 the parity data in the first area.